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ART UNIT	PAPER NUMBER
2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,123	GLEN, DAVID I. J.	
	Examiner	Art Unit	
	Javid A Amini	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☒ Claim(s) 1-32 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 5-6, 9, 12-14 and 17 rejected under 35 U.S.C. 102(e) as being anticipated by Blinn US patent 6,184,891 B1.

2. Claim 1.

As for claim 1, "A video graphics module comprises: a plurality of video graphics pipelines, wherein each of the plurality of video graphics pipelines is operable to process a corresponding image layer and wherein one of the plurality of video graphics pipelines processes a foremost image layer; and a blending module operably coupled to the plurality of video graphics pipelines, wherein the blending module blends, in accordance with a blending convention, the corresponding image layers in a predetermined blending order to produce an output image having the foremost image layer blended in a foremost position with respect to the other corresponding image layers with negligible loss of information of the other corresponding image layers", Blinn discloses in (col.17, lines 53-57) that in a layered graphics pipeline, the rasterizer can apply fog to each object independently as it renders the object to a sprite layer. The compositing buffer can then be used to composite fogged object layers and the opaque fog background layer. Blinn illustrates in Figs. 2, 4-6 the plurality of video graphics pipelines processes a foremost image layer and a blending module operably coupled to the plurality of

video graphics pipelines. Blinn teaches the layers of image in Figs. 4-6, each layer can be text or color graphics. The interpretation between applicant's invention that is shown in Fig. 1 with Blinn's Fig. 4 are as follows: consider "A", "B" and "Fog" in Fig. 4 the "bike picture", the text of "classic bike" and the price tag of "$99" respectively in applicant's Fig. 1. The image of Fog (Blinn: Fig. 4) is the foremost image layer that is equivalent of the price tag of "$99" of applicant's Fig.1. Blinn discloses in Fig. 4 that is corresponding image layers with negligible loss of information of the other corresponding image layers.

3. Claim 2.

As for claim 2, "The video graphics module of claim 1, wherein the blending convention further comprises at least one of AND/XOR blending and alpha blending", Blinn discloses in (col. 2, lines 34-41) that the blend unit 24 includes logic to combine partially transparent pixel values (negligible loss of information, sometimes called pixel fragments) at a pixel location into a final output pixel. Some architectures also rasterize geometric primitives at a subpixel resolution and then blend the pixel values of the subpixels in the neighborhood of each pixel location to compute final pixel values at each pixel location.

4. Claim 3.

As for claim 3, "The video graphics module of claim 2, wherein the alpha blending further comprises a specified per pixel alpha value or a global alpha value, wherein the alpha blending is performed using one of a plurality of pixel depths", Blinn discloses in (col. 2, lines 14-25) that the blend unit 24 determines whether an input pixel generated by the rasterizer occludes a previously generated pixel in the frame buffer at the same pixel location. If it does, the blend unit 24 replaces the pixel in the frame buffer with the new pixel. If it does not, the blend unit 24 discards the new pixel. An alternative technique is to sort the polygons in depth order and rasterize them in front to back order. The depth value of pixel is interpreted as Z-direction or

third dimension. (Definition of alpha blending is: it combines a transparent source color with a translucent destination color.)

5. Claim 5.

As for claim 5, "The video graphics module of claim 1, wherein the predetermined blending order further comprises blending at least two of the corresponding image layers to produce an intermediate blended image, and subsequently blending the foremost image layer with the intermediate blended image", Blinn teaches in (col. 6, lines 23-30) that fogged pixels from different surfaces can be combined in back-to-front (intermediate to subsequently) order using the over operator.

6. Claim 6.

As for claim 6, "The video graphics module of claim 1, wherein the blending module further comprises a first mixing module and a second mixing module, wherein the first mixing module blends at least two of the corresponding image layers to produce an intermediate blended image, and wherein the second mixing module blends the foremost image layer with the intermediate blended image", Blinn illustrates in Fig. 8 a gsprite engine that comprises of alpha buffer (first mixing module) and color buffer (second mixing modules) and so on. This engine blends the corresponding image layers (back-front) to produce an intermediate/foremost image layers.

7. Claim 9.

As for claim 9, "The video graphics module of claim 1, wherein each of the corresponding image layers has a color base of at least one of: an RGB color base and a YUV color base", Blinn teaches in (col. 16, lines 12-13) that the resolved pixels have RGB color and alpha components. But Blinn dose not explicitly specify the YUV color base, however Snyder illustrates in Fig. 4A the color buffer that stores the YUV color base.

8. Claim 12.

As for claim 12, "A video graphics module comprises: a video graphics pipeline module operable to process at least one image layer; a hardware cursor pipeline operable to process a cursor image; and a blending circuit operably coupled to the video graphics pipeline and the hardware cursor pipeline, wherein the blending module blends, in accordance with a blending convention, the at least one image layer and the cursor image to produce an output image having the cursor image alpha blended with the at least one corresponding image layer", Blinn discloses in (col.17, lines 53-57) that in a layered graphics pipeline, the rasterizer can apply fog to each object independently as it renders the object to a sprite layer. The compositing buffer can then be used to composite fogged object layers and the opaque fog background layer. Blinn illustrates in Figs. 2, 4-6 the plurality of video graphics pipelines processes a foremost image layer and a blending module operably coupled to the plurality of video graphics pipelines. Blinn teaches the layers of image in Figs. 4-6, each layer can be text or color graphics. The interpretation between applicant's invention that is shown in Fig. 1 with Blinn's Fig. 4 are as follows: consider "A", "B" and "Fog" in Fig. 4 the "bike picture", the text of "classic bike" and the price tag of "$99" respectively in applicant's Fig. 1. The image of Fog (Blinn: Fig. 4) is the foremost image layer that is equivalent of the price tag of "$99" of applicant's Fig.1. Blinn discloses in Fig. 4 that is corresponding image layers with negligible loss of information of the other corresponding image layers.

9. Claim 13.

As for claim 13, "The video graphics module of claim 12, wherein the blending convention further comprises at least one of: AND/XOR blending and alpha blending", Blinn discloses in (col. 2, lines 34-41) that the blend unit 24 includes logic to combine partially transparent pixel values (negligible loss of information, sometimes called pixel fragments) at a pixel location into

a final output pixel. Some architectures also rasterize geometric primitives at a subpixel resolution and then blend the pixel values of the subpixels in the neighborhood of each pixel location to compute final pixel values at each pixel location.

10. Claim 14.

As for claim 14, "The video graphics module of claim 13, wherein the alpha blending further comprises a specified per pixel alpha value or a global alpha value, wherein the alpha blending is performed using one of a plurality of pixel depths", Blinn discloses in (col. 2, lines 14-25) that the blend unit 24 determines whether an input pixel generated by the rasterizer occludes a previously generated pixel in the frame buffer at the same pixel location. If it does, the blend unit 24 replaces the pixel in the frame buffer with the new pixel. If it does not, the blend unit 24 discards the new pixel. An alternative technique is to sort the polygons in depth order and rasterize them in front to back order. The depth value of pixel is interpreted as Z-direction or third dimension. (Definition of alpha blending is: it combines a transparent source color with a translucent destination color.)

11. Claim 17.

As for claim 17, "The video graphics module of claim 16, wherein the blending circuit further comprises a first mixing module and a second mixing module, wherein the first mixing module blends the at least two of the plurality of image layers to produce the intermediate blended image, and wherein the second mixing module blends the cursor image layer with the intermediate blended image", Blinn illustrates in Fig. 8 a gsprite engine that comprises of alpha buffer (first mixing module) and color buffer (second mixing modules) and so on. This engine blends the corresponding image layers (back-front) to produce an intermediate/foremost image layers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4, 10-11, 15, 20-27 and 28-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Blinn, and further in view of Snyder et al. US patent 6,326,964 B1.

13. Claim 4.

As for claim 4, "The video graphics module of claim 2, wherein the AND/XOR blending further comprises one of a plurality of pixel depths", Blinn dose not explicitly specify the AND/XOR, however Snyder teaches in Fig. 13 that the compositing logic 482 is responsible for calculating the pixel values as they are written into the scanline buffer. This is accomplished by performing a blending operation between the pixel value that is currently stored in the scanline buffer and the one that is being written to the compositing buffer. In one implementation, the compositing logic performs four parallel pixel operations per clock cycle.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

14. Claim 10.

As for claim 10, "The video graphics module of claim 9, wherein the one of the plurality of video graphics pipelines that is processing the foremost image layer produces a first foremost image layer having the RGB color base and a second foremost image layer having the YUV

color base", the step is obvious because when an image is considered as a 2D (x and y buffer) and as a 3D (z-buffer/pixel depth) should have the RGB and YUV color base respectively.

15. Claim 11.

As for claim 11, "The video graphics module of claim 9, wherein the plurality of video pipelines processes the corresponding image layers to have the RGB color base, and wherein the blending module further comprises: an RGB blending module operably coupled to produce the output image having the RGB color base; an RGB to YUV conversion module operably coupled to convert corresponding image layers to have the YUV color base, and a YUV blending module operably coupled to produce the output image having the YUV color base from the corresponding image layers having the YUV color base", Blinn dose not explicitly specify the conversion of color bases, however Snyder teaches in (col. 44, lines 60-61) that converts the RGB data input to a YUV-like luminance-chrominance system (optional). Snyder teaches in (col. 45, lines 13-44) that converts the colors in the YUV-like luminance-chrominance system to RGB colors, if the compression process included the corresponding optional step. The flow diagram is illustrated by Snyder in Fig. 6 an overview of the display generation process of an embodiment. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

16. Claim 15.

As for claim 15, "The video graphics module of claim 13, wherein the AND/XOR blending further comprises one of a plurality of pixel depths", Blinn dose not explicitly specify the AND/XOR, however Snyder teaches in Fig. 13 that the compositing logic 482 is responsible for calculating the pixel values as they are written into the scanline buffer. This is accomplished by

performing a blending operation between the pixel value that is currently stored in the scanline buffer and the one that is being written to the compositing buffer. In one implementation, the compositing logic performs four parallel pixel operations per clock cycle.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

17. Claim 16.

As for claim 16, "The video graphics module of claim 12, wherein the at least one image layer includes a plurality of image layers, wherein the blending circuit blends the plurality of images layers and the cursor image layer in a predetermined blending order, wherein the predetermined blending order further comprises blending at least two of the plurality of image layers to produce an intermediate blended image, and subsequently blending the cursor image layer with the intermediate blended image", Blinn teaches in (col. 6, lines 23-30) that fogged pixels from different surfaces can be combined in back-to-front (intermediate to subsequently) order using the over operator.

18. Claim 20.

As for claim 20, "The video graphics module of claim 12, wherein the blending circuit further comprises: a first input for receiving the at least one image layer; a second input for receiving the cursor image layer; and blending module operable to alpha blend the at least one image layer and the cursor image layer to produce the output image", Blinn dose not explicitly specify a first/second inputs to receive image layers, however, Snyder illustrates in Fig. 2 that the input device(s) 140 can include a keyboard, cursor positioning device such as a mouse, joysticks, as well as a variety of other commercially available input devices.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

19. Claim 21.

As for claim 21 "The video graphics module of claim 12, wherein the at least one image layer and the cursor image each has a color base of at least one of an RGB color base and a YUV color base", Blinn teaches in (col. 16, lines 12-13) that the resolved pixels have RGB color and alpha components. But Blinn dose not explicitly specify the YUV color base, however Snyder illustrates in Fig. 4A the color buffer that stores the YUV color base.

20. Claim 22.

As for claim 22, "The video graphics module of claim 21, wherein the hardware cursor pipeline produces a first cursor image having the RGB color base and a second cursor image having the YUV color base", the step is obvious because when an image is considered as a 2D (x and y buffer) and as a 3D (z-buffer/pixel depth) should have the RGB and YUV color base respectively.

21. Claim 23.

As for claim 23"The video graphics module of claim 21, wherein the video pipeline processes the at least one image layer to have the RGB color base, wherein the hardware cursor pipeline processes the cursor image to have the RGB color base, and wherein the blending module further comprises: an RGB blending module operably coupled to produce the output image having the RGB color base; an RGB to YUV conversion module operably coupled to convert the at least one image layer and the cursor image to each have the YUV color base, and a YUV blending module operably coupled to produce the output image having the YUV color base from the at

least one image layer having the YUV color base and the cursor image having the YUV color base", Blinn dose not explicitly specify the conversion of color bases, however Snyder teaches in (col. 44, lines 60-61) that converts the RGB data input to a YUV-like luminance-chrominance system (optional). Snyder teaches in (col. 45, lines 13-44) that converts the colors in the YUV-like luminance-chrominance system to RGB colors, if the compression process included the corresponding optional step. The flow diagram is illustrated by Snyder in Fig. 6 an overview of the display generation process of an embodiment.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

22. Claim 24.

As for claim 24, "An apparatus for determining an alpha calculation mode, the apparatus comprises: a processing module; and memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to (a) determine an alpha blending mode; (b) obtaining blending information based on the alpha blending mode; (c) generating a corresponding blending value based on the blending information; and (d) providing the corresponding blending value to a blending module", Blinn dose not explicitly specify the terms in claim 24, however, Snyder illustrates in Fig. 5B that the image preprocessor then queues the chunk data for tiling. Tiling refers to the process of determining pixel values such as color and alpha for pixel locations covered or partially covered by one or more polygons. The steps of providing/generating/obtaining blending information/value are obvious because in order to generate and provide the corresponding blending value to a blending module, the blending information based on the alpha mode must be obtained.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

23. Claim 25.

As for claim 25 "The apparatus of claim 24, wherein the memory further comprises operational instructions that cause the processing module to, when the alpha blending mode indicates using a global alpha blending value, retrieve at least one global alpha value from a general alpha register", the step is obvious because the memory is a place of storage for operational instructions (global/general alpha blending values) that causes the processing to retrieve and to transmit from or to the next stage.

24. Claim 26.

As for claim 26, "The apparatus of claim 24, wherein the memory further comprises operational instructions that cause the processing module to, when the alpha blending mode indicates using a per pixel alpha blending value, retrieve at least one corresponding per pixel alpha blending value from an image layer input", the step is obvious because the memory is a place of storage for operational instructions (global/general alpha blending values) that causes the processing to retrieve and to transmit from or to the next stage.

25. Claim 27.

As for claim 27, "The apparatus of claim 24, wherein the memory further comprises operational instructions that cause the processing module to, when the alpha blending mode indicates using a key alpha blending value, retrieve an alpha key indication from a keyer, wherein the keyer generates the alpha key indication from at least one corresponding per pixel alpha value associated with an image layer input", the step is obvious because the memory is a place of

storage for operational instructions (alpha key blending values) that causes the processing to retrieve and to transmit from or to the next stage.

26. Claim 28.

As for claim 28, "A video graphics data blending circuit comprises: a first input for receiving a first image layer; a second input for receiving a second image layer: a blending module operably coupled to blend the first and second image layers based on an alpha calculation using a specified alpha value; and an alpha value calculation module operably coupled to the blending module, wherein the alpha value calculation module generates the specified alpha valued based on at least one of: a global alpha value, a per pixel value associated with at least one of the first and second image layers, and a non-alpha blend mode", Blinn dose not explicitly specify the terms in claim 28, however, Snyder illustrates in Fig. 5B that the image preprocessor then queues the chunk data for tiling. Tiling refers to the process of determining pixel values such as color and alpha for pixel locations covered or partially covered by one or more polygons. The steps of providing/generating/obtaining blending information/value are obvious because in order to generate and provide the corresponding blending value to a blending module, the blending information based on the alpha mode must be obtained. The steps of "a global alpha value" and "non-alpha blend mode" are obvious because the memory is a place of storage for operational instructions (global/non-alpha blending values) that causes the processing to retrieve and to transmit from or to the next stage.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

27. Claim 29.

As for claim 29, "The video graphics data blending circuit of claim 28, wherein the alpha value calculation module further comprises firmware that, for the non-alpha blend mode, detects a color key in at least one of the first and second image layers to produce a color key result, and generates the specified alpha value as a fully transparent value or a fully opaque value based on the color key result", Blinn dose not explicitly specify the terms in claim 24, however, Snyder illustrates in Fig. 5B that the image preprocessor then queues the chunk data for tiling. Tiling refers to the process of determining pixel values such as color and alpha for pixel locations covered or partially covered by one or more polygons. The steps of calculating, detecting and generating alpha information/value are obvious because in order to generate and provide the corresponding blending value to a blending module, the blending information based on the alpha mode must be obtained.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Snyder into Blinn in order to improve the degree of compression and the color space conversion applies to each pixel independently and does not change the value of alpha (see Snyder, col. 45, line 18-25).

28. Claim 30.

As for claim 30, "The video graphics data blending circuit of claim 28, wherein the blending module further comprises firmware for performing the blending of the first and second image layers using a premultiplied alpha blending process or a non-premultiplied alpha blending process", the step is obvious because in order to determine the blending process, firmware should have the information of premultiplied and non-premultiplied alpha blending.

29. Claim 31.

As for claim 31, "The video graphics data blending circuit of claim 28 further comprises a first multiplexer operably coupled to the first input and a second multiplexer operably coupled to the second input, wherein the first multiplexer is operably coupled to receive a plurality of image layers and to output the first image layer and the second multiplexer is operably coupled to receive the plurality of image layers and output the second image layer", the step is obvious because in order to transmit and receive several different streams of data over a common communications line. Multiplexer are used either to attach many communications lines to a smaller number of communications ports or to attach a large number of communications ports to a smaller number of communications lines. See also rejection of claim 28.

30. Claim 32.

As for claim 32, "The video graphics data blending circuit of claim 31, wherein the alpha value calculation module further comprises firmware that provides control information to the first and second multiplexers such that the first multiplexor outputs the first image layer and the second multiplexor outputs the second image layer", see rejection of claim 31.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

31. Claims 1-32 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

32. Claims 3, 7, 18, 25 and 28 recite the limitation "global". There is insufficient antecedent basis for this limitation in the claim.

33. Claims 7 and 18 recite the limitation " one of the at least two of the corresponding image layers " in claims 7 and 18. There is insufficient antecedent basis for this limitation in the claim.

34. Claims 7 and 18 recite the limitation " blending and alpha values" in claims 7 and 18. There is insufficient antecedent basis for this limitation in the claim. According to the definition of alpha blending, the fig. 1 dose not show the transparency. It is illustrating an overlapped.

35. (Definition of alpha blending: it combines a transparent source color with a translucent destination color.)

36. Claims 8 and 19 recites the limitation " a first input for receiving the intermediate blended image; a second input for receiving the foremost image layer" in claims 8 and 19. There is insufficient antecedent basis for this limitation in the claim to illustrates how the detection of intermediate blended image and the foremost image layer take a place.

37. Claims 1-24 and 28-30 recite the limitation "module". There is insufficient antecedent basis for this limitation in the claim. The applicant should specify clearly the content of this module.

38. Claims 5 and 16 recite the limitation "predetermined". There is insufficient antecedent basis for this limitation in the claim.

39. Claim 24 recites the limitation "determining". There is insufficient antecedent basis for this limitation in the claim.

40. Claims 7, 24, 28 and 29 recite the limitation "calculation mode". There is insufficient antecedent basis for this limitation in the claim.

41. Claims 24 and 28-29 recite the limitation "generating/generates". There is insufficient antecedent basis for this limitation in the claim.

42. Claim 24 recites the limitation "obtaining/providing". There is insufficient antecedent basis for this limitation in the claim.

43. Claim 25 recites the limitation "general". There is insufficient antecedent basis for this limitation in the claim.

44. Claims 25-27 recite the limitations "retrieve/operational instruction". There is insufficient antecedent basis for this limitation in the claim.

45. Claims 27 and 29 recite the limitation "alpha key". There is insufficient antecedent basis for this limitation in the claim.

46. Claims 28-32 recite the limitation "circuit". There is insufficient antecedent basis for this limitation in the claim.

47. Claims 7, 8 18-20 and 28 recite the limitations "first and second inputs". There is insufficient antecedent basis for this limitation in the claim.

48. Claims 18, and 28-29 recite the limitation "non-alpha". There is insufficient antecedent basis for this limitation in the claim.

49. Claims 29-32 recite the limitation "firmware". There is insufficient antecedent basis for this limitation in the claim.

50. Claim 29 recite the limitation "detect". There is insufficient antecedent basis for this limitation in the claim.

51. Claims 3, 14 and 30 recite the limitation "performing". There is insufficient antecedent basis for this limitation in the claim.

52. Claim 30 recite the limitations "premultiplied/non-premultiplied". There is insufficient antecedent basis for this limitation in the claim.

53. Claims 18-20 and 31 recite the limitation "receive". There is insufficient antecedent basis for this limitation in the claim.

54. Claims 24-27 recite the limitation "memory". There is insufficient antecedent basis for this limitation in the claim.

55. Claims 11, 23 recite the limitation "conversion". There is insufficient antecedent basis for this limitation in the claim.

56. Claims 9-11 and 21-23 recite the limitation "color base". There is insufficient antecedent basis for this limitation in the claim.

57. Claims 12, 17, 19 and 22 recite the limitation "cursor". There is insufficient antecedent basis for this limitation in the claim.

58. Claim 12 recites the limitation "hardware". There is insufficient antecedent basis for this limitation in the claim.

59. Claims 1, 4, 13, 15 recite the limitations "AND/XOR". There is insufficient antecedent basis for this limitation in the claim.

60. Claims 3, 6-7 and 17 recite the limitation "mixing". There is insufficient antecedent basis for this limitation in the claim.

61. Claims 1, 5-6, 8 and 10 recite the limitation "foremost". There is insufficient antecedent basis for this limitation in the claim.

62. Claim 1 recites the limitation "negligible". There is insufficient antecedent basis for this limitation in the claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-8705 for regular communications and 703-746-8705 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Javid Amini
January 16, 2003

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
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